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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,728	11/06/2001	Mohammad A. Abdallah	42390P5943C	2359

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/005,728	ABDALLAH ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,18,21-24 and 39-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23 and 24* is/are allowed.

6)☒ Claim(s) *16,18,21,22,39-41,43 and 44* is/are rejected.

7)☒ Claim(s) *42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/9/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 16, 18, 21-24, and 39-44 are presented for examination.

2. It is noted that claims 17, 26-31, and 33-37 were canceled in paper number 20070208, mailed February 12, 2007.

3. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a)shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

6. Claims 39-41 are rejected under 35 USC § 102(e) as being anticipated by Van Hook et al, U.S. Patent 5,734,874.

Van Hook et al. taught (e.g. see figs. 1-11b) the invention as claimed (as per claim 39), including a data processing ("DP") system comprising:

A. a processor (fig. 1) comprising;

B. decode logic (46) to decode a packed sum of absolute differences (PSAD) (fig. 9a, 138, PDIST) instruction having a first format (fig. 9a) to identify a first set of packed data ($freg_{rs1}$), said decode logic to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction, the first set of operations comprising;

C. a packed subtract and write carry (PSUBWC) operation (fig. 9b, 57a ... 57h, upper 8

bit subtracters each write a carry to lines connecting to 59a ... 59h);

D. a packed absolute value and read carry (PABSRC) operation (59a ... 59h, multiplexers read carry from subtracters and generate multiple absolute values); and,

E. a packed add horizontal (PADDH) operation (61a, 61b, 61c, 62, 65, 63a, consuming eight 8-bit values and producing a sum in 63b); and,

F. execution logic to perform the first set of operations initiated by the decode logic (fig. 1, 28, fig. 9b (which is a component of element 28 of fig. 1).

7. As to claim 40, Van Hook et al. taught that the first format (fig. 9a) identified the first set of packed data as packed bytes (fig. 9b, "byte slice 0" ... "byte slice 7").

8. As to claim 41, Van Hook et al. taught that performing the PSUBWC operation caused the execution logic to:

subtract one (57a, upper subtracter, left side input) of a plurality of elements ("byte slice 0" ... "byte slice 7") of a first packed data (fig. 6a, 66a) of the first set of packed data (fig. 9a, $freg_{rs1}$) from a corresponding one (57a, right side input) of a plurality of elements of a second packed data (fig. 9a, $freg_{rs2}$) to produce a first result having a plurality of difference elements (output of subtracter) and a plurality of sign indicators (carry output of subtracter); and,

store the plurality of difference elements and the plurality of sign indicators (the outputs of the subtracters are stored to the multiplexers 59a ... 59h).

9. Claims 43-44 are rejected under 35 USC § 103 as being unpatentable over Van Hook et al., U.S. Patent 5,734,874, in view of Lee, U.S. Patent 5,721,697.

10. As to claim 43, Van Hook et al. did not teach performing the PADDH operation utilizing a multiplier as claimed by the claim. However, Lee taught:

A. produce a first plurality of partial products in a multiplier having a plurality of partial product selectors (col. 2 lines 21-26);

B. insert an element of a first plurality of elements of a first packed data into and

substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; (col. 5 lines 35-56 and table 5); and,

C. add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements (table 5, "ZZZZZ" is the result, see col. 5 lines 54-55);

D. the field having a least significant bit (The rightmost Z of the element "ZZZZZ" is the least significant bit; also note that all numbers have both a least and most significant digit).

11. As to claim 44, Lee taught shifting the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result (col. 5 lines 55-56).

12. Claim 16 is rejected under 35 USC § 102(e) as anticipated by Yung, U.S. Patent 5,996,066, or, in the alternative, under 35 USC 103 as obvious over Yung in view of Van Hook et al., U.S. Patent 5,734,874.

13. Under anticipation, Yung taught:

A. a processor (fig. 1) comprising;

B. a decode unit (46) to decode (col. 4 lines 40-41) to decode a plurality of packed data instructions (col. 2 lines 7-45) including a packed sum of absolute differences (PSAD) instruction (col. 5 lines 25-27, "pixel distance") having a first format (fig. 6b) to identify a first set of packed data (RS1), and

C. a packed multiply-add (PMAD) instruction (col. 2 lines 10-14) having a second format (fig. 6b) to identify a second set of packed data (RS1),

D. said decode unit to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction (col. 5 lines 27-28) and to initiate a second set of operations on the second set of packed data responsive to decoding the

PMAD instruction (col. 5 lines 28-29); and,

E. an execution unit (28) to perform a first operation of the first set of operations initiated by the decode unit and to perform a second operation of the second set of operations initiated by the decode unit (col. 4 lines 40-55).

14. Under obviousness, although Yung taught a pixel distance computation unit (fig. 5, 56), Yung relied upon one of ordinary skill in the art to know that "pixel distance" was defined as "a packed sum of absolute differences (PSAD)" operation. Accordingly, Yung did not teach explicitly that "pixel distance" was defined as "packed sum of absolute differences". However, Van Hook et al. taught that "pixel distance" was defined as "packed sum of absolute differences" (col. 10 lines 53-64). One of ordinary skill in the art, lacking knowledge of the definition of "pixel distance" in Yung's disclosure, would have been motivated to investigate the meaning of pixel distance within the art. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Van Hook et al. into Yung because Van Hook et al. provided not only illumination as to the definition of "pixel distance" in Yung's disclosure, but additionally provided a circuit diagram of a system to compute a "pixel distance" operation (fig. 9b). Furthermore, Van Hook et al. specifically indicated that his disclosure was applicable to graphics processing (col. 2 lines 14-26) which was an environment within which Yung disclosed that his invention was applicable (col. 1 line 65 to col. 2 line 6). Additionally, it is noted that figs. 1-6b of both Yung and Van Hook et al. are identical and that both patents are assigned to Sun Microsystems, Inc. Additionally, Yung is the third named inventor on the Van Hook et al. patent.

15. Claim 18 is rejected under 35 USC 103 as being unpatentable over Yung, in view of Van Hook et al., as detailed, supra.

16. As to claim 18, Van Hook et al. taught the first set of operations comprising;

A. a packed subtract and write carry (PSUBWC) operation (fig. 9b, 57a ... 57h, upper 8 bit subtracters each write a carry to lines connecting to 59a ... 59h);

B. a packed absolute value and read carry (PABSRC) operation (59a ... 59h, multiplexers

read carry from subtracters and generate multiple absolute values); and,

C. a packed add horizontal (PADDH) operation (61a, 61b, 61c, 62, 65, 63a, consuming eight 8-bit values and producing a sum in 63b).

17. Claims 21-22 are rejected under 35 USC § 103 as being unpatentable over Yung in view of Van Hook et al. and further in view of Lee, U.S. Patent 5,721,697.

18. As to claim 21, Van Hook et al. did not teach performing the PADDH operation utilizing a multiplier as claimed by the claim. However, Lee taught:

A. produce a first plurality of partial products in a multiplier having a plurality of partial product selectors (col. 2 lines 21-26);

B. insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; (col. 5 lines 35-56 and table 5); and,

C. add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements (table 5, "ZZZZZ" is the result, see col. 5 lines 54-55);

D. the field having a least significant bit (The rightmost Z of the element "ZZZZZ" is the least significant bit; also note that all numbers have both a least and most significant digit).

19. As to claim 22, Lee taught shifting the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result (col. 5 lines 55-56).

20. Claims 23-24 are allowable over the prior art of record.

21. Claim 42 is objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims,

and the objected claim.

22. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
May 29, 2007

RICHARD L. ELLIS
PRIMARY EXAMINER